

Fig. 1 Prior art

10064211.062102

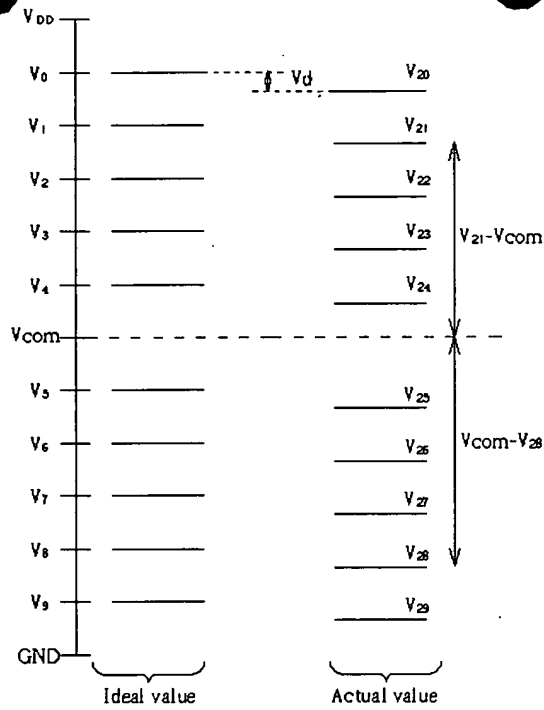


Fig. 2 Prior art

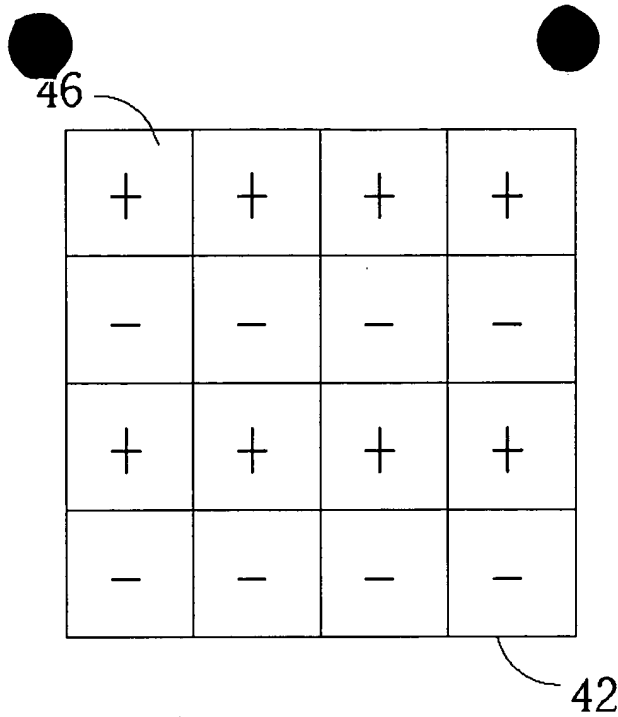


Fig. 3A Prior art

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-	-	-	-
+	+	+	+
-	-	-	-
+	+	+	+

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Fig. 3B Prior art

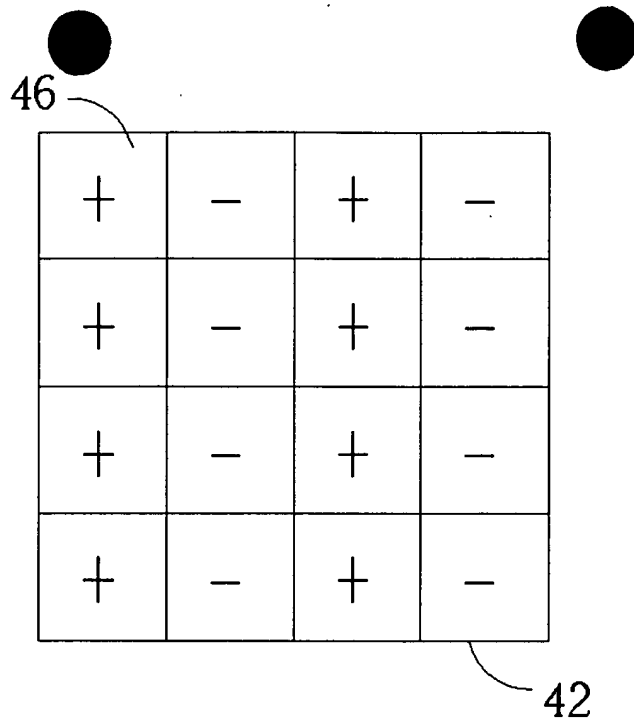


Fig. 4A Prior art

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**SECRET**

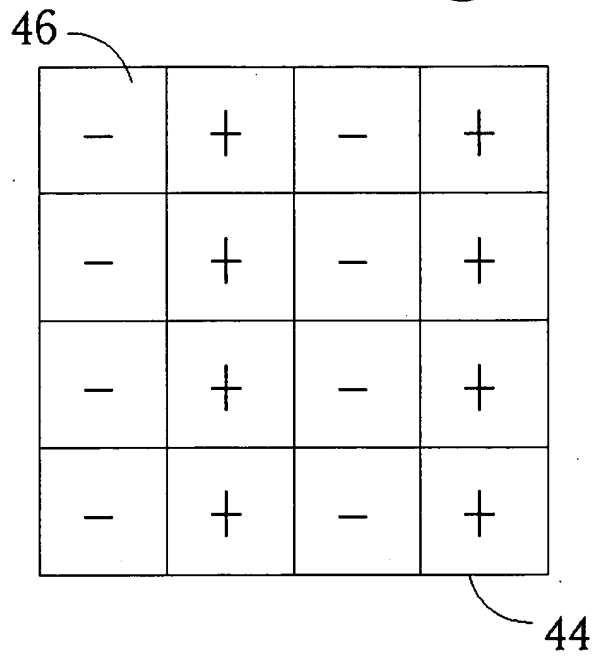


Fig. 4B Prior art

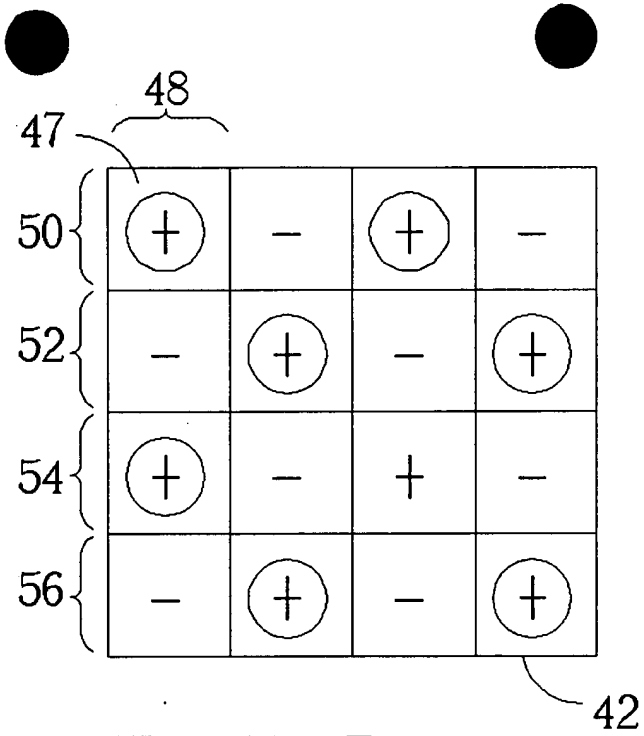


Fig. 5A Prior art

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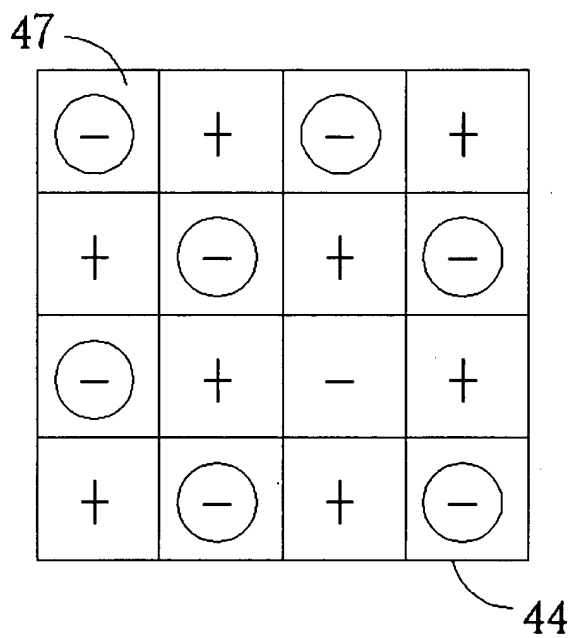


Fig. 5B Prior art



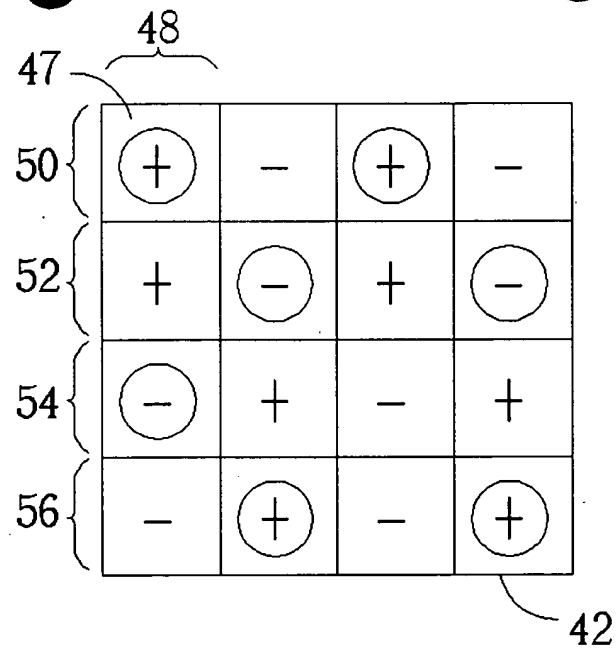


Fig. 6A Prior art

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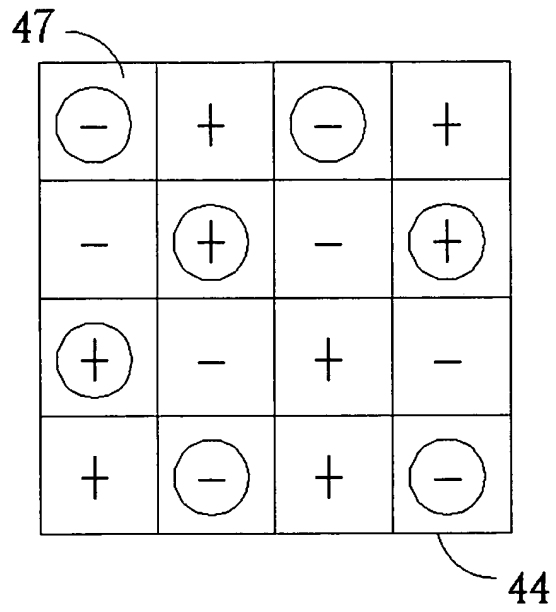


Fig. 6B Prior art

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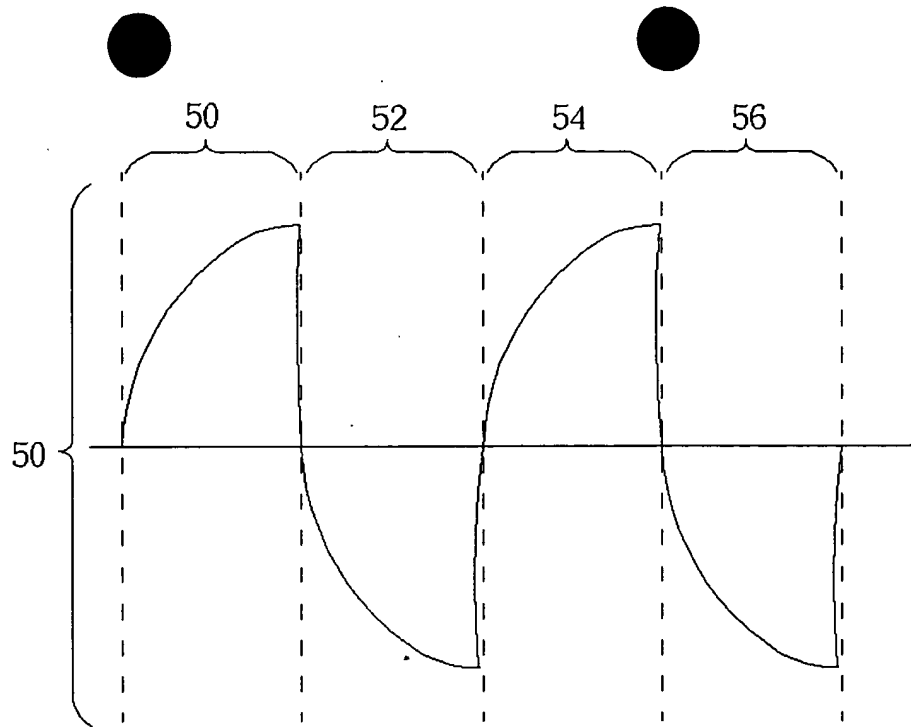


Fig. 7 Prior art

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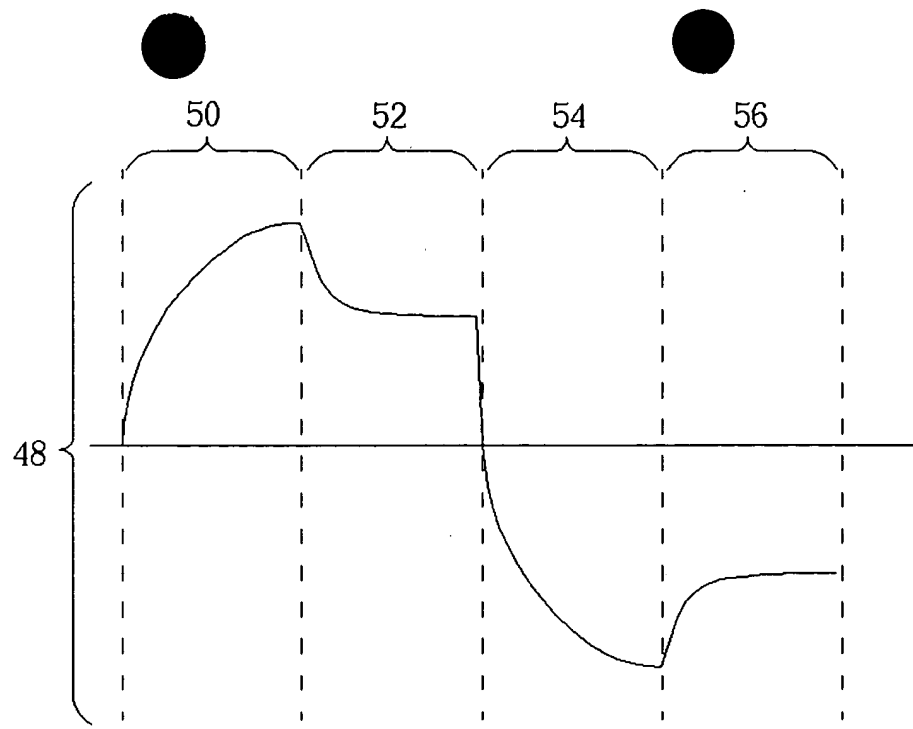


Fig. 8 Prior art

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Detector

Logic circuit

Controller

Positive buffer circuit

Negative buffer circuit

Polarity signal

Horizontal synchronization signal

First latch circuit

Second latch circuit

Precharge circuit

Output buffer

Precharge circuit

Output buffer

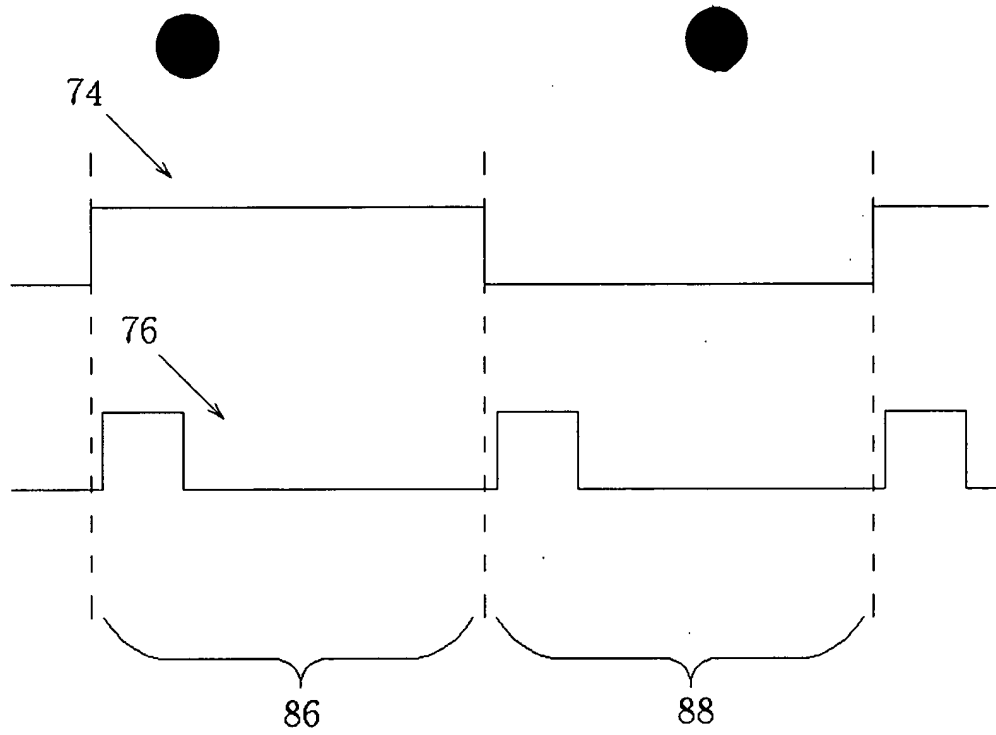


Fig. 10 Prior art

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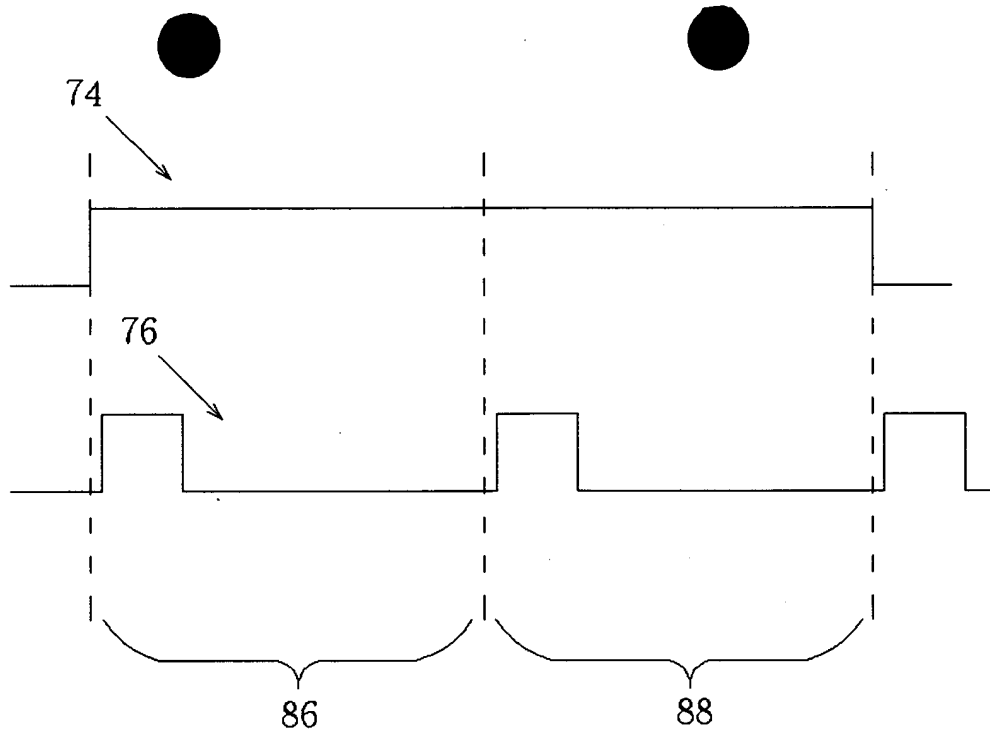


Fig. 11 Prior art

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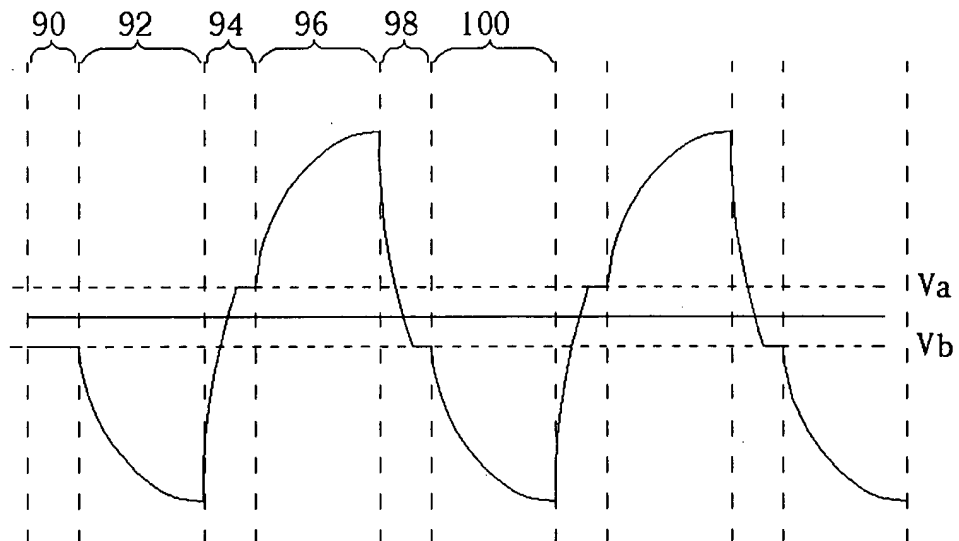


Fig. 12

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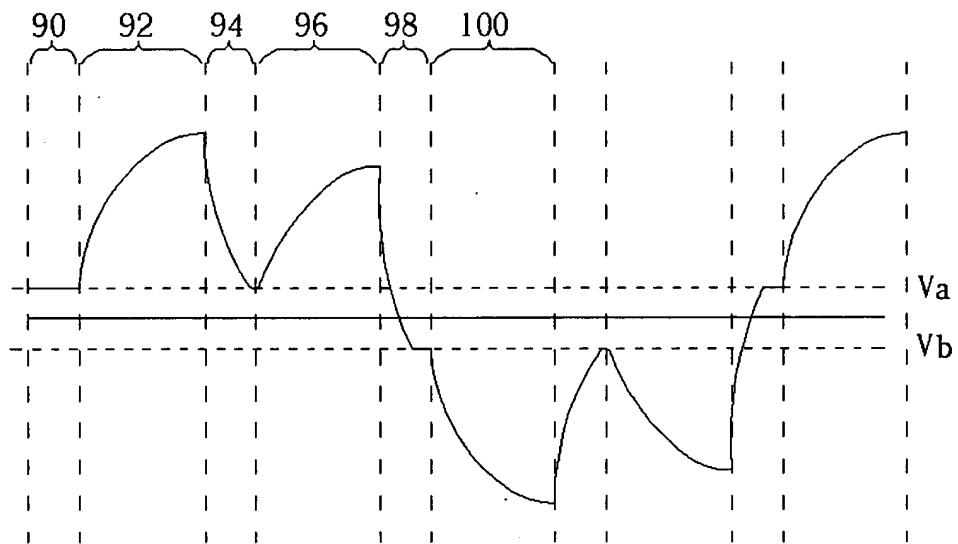


Fig. 13

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